

FDMJ1023PZ

Dual P-Channel PowerTrench® MOSFET

-20V, -2.9A, 112mΩ

Features

- Max $r_{DS(on)}$ = 112mΩ at $V_{GS} = -4.5V$, $I_D = -2.9A$
- Max $r_{DS(on)}$ = 160mΩ at $V_{GS} = -2.5V$, $I_D = -2.4A$
- Max $r_{DS(on)}$ = 210mΩ at $V_{GS} = -1.8V$, $I_D = -2.1A$
- Max $r_{DS(on)}$ = 300mΩ at $V_{GS} = -1.5V$, $I_D = -1.0A$
- Low gate charge, high power and current handling capability
- HBM ESD protection level > 1.5kV typical (Note 3)
- RoHS Compliant

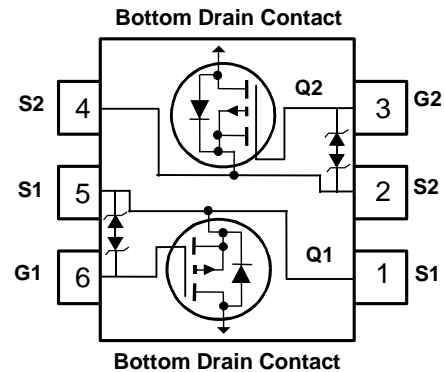
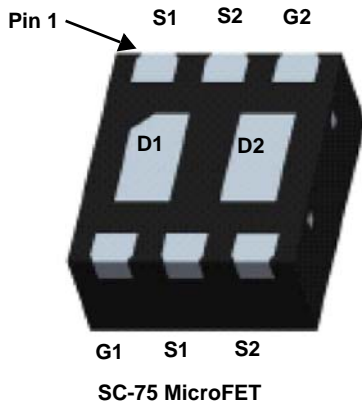


General Description

This dual P-Channel MOSFET uses Fairchild's advanced low voltage PowerTrench® process. This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible. The SC-75 MicroFET package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Applications

- Battery management/charger application



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current -Continuous	(Note 1a)	-2.9
	-Pulsed		-12
P_D	Power Dissipation	(Note 1a)	1.4
	Power Dissipation	(Note 1b)	0.7
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	89	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	182	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
023	FDMJ1023PZ	SC-75 MicroFET	7"	8mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{V}$, $V_{GS} = 0\text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{V}$, $V_{DS} = 0\text{V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$	-0.4	-0.7	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		2.3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{V}$, $I_D = -2.9\text{A}$		93	112	m Ω
		$V_{GS} = -2.5\text{V}$, $I_D = -2.4\text{A}$		128	160	
		$V_{GS} = -1.8\text{V}$, $I_D = -2.1\text{A}$		173	210	
		$V_{GS} = -1.5\text{V}$, $I_D = -1.0\text{A}$		217	300	
		$V_{GS} = -4.5\text{V}$, $I_D = -2.9\text{A}$, $T_J = 125^\circ\text{C}$		130	160	
g_{FS}	Forward Transconductance	$V_{DD} = -5\text{V}$, $I_D = -2.9\text{A}$		7		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		300	400	pF
C_{oss}	Output Capacitance			55	75	pF
C_{rss}	Reverse Transfer Capacitance			45	70	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{V}$, $I_D = -2.9\text{A}$ $V_{GS} = -4.5\text{V}$, $R_{GEN} = 6\Omega$		5	10	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns
t_f	Fall Time			12	22	ns
Q_g	Total Gate Charge			4.6	6.5	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = -5\text{V}$, $I_D = -2.9\text{A}$ $V_{GS} = -4.5\text{V}$		0.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.0		nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain-Source Diode Forward Current			-1.1	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = -1.1\text{A}$		-0.9	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -2.9\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$		28	45	ns
Q_{rr}	Reverse Recovery Charge			15	27	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in}$. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. $89^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper



b. $182^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

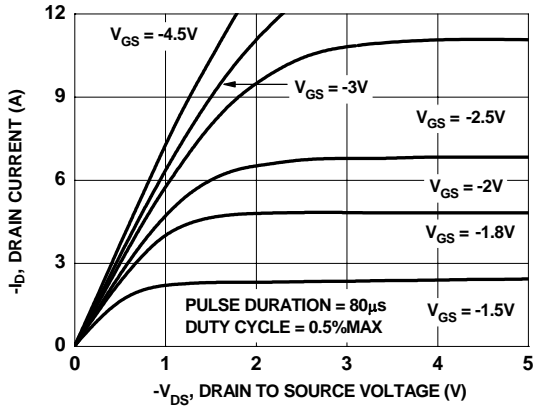


Figure 1. On-Region Characteristics

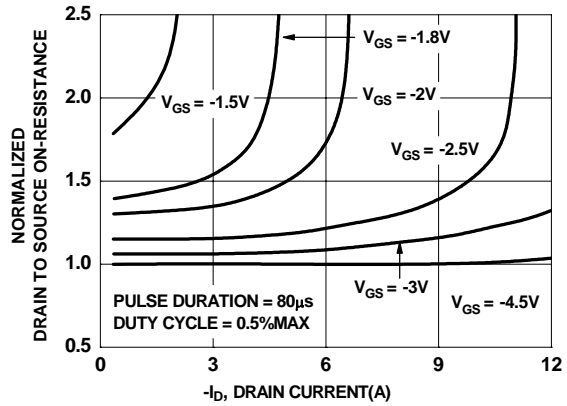


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

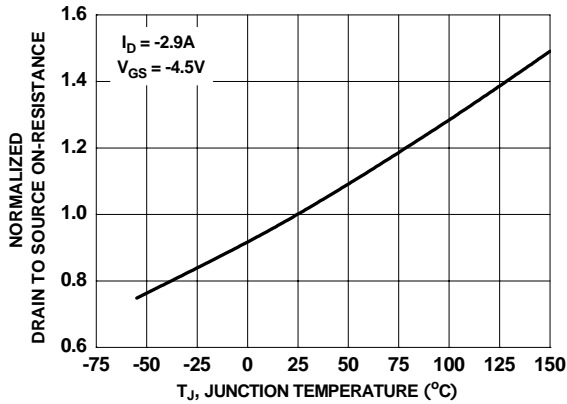


Figure 3. Normalized On-Resistance vs Junction Temperature

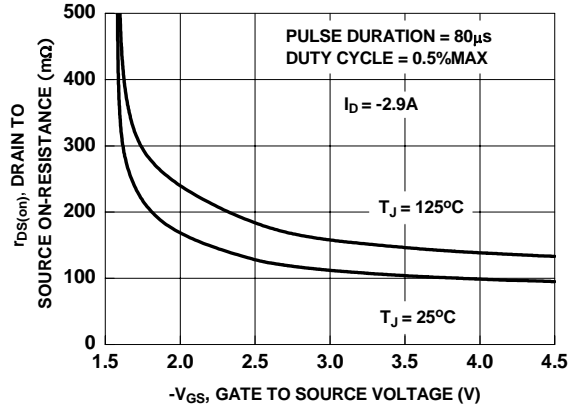


Figure 4. On-Resistance vs Gate to Source Voltage

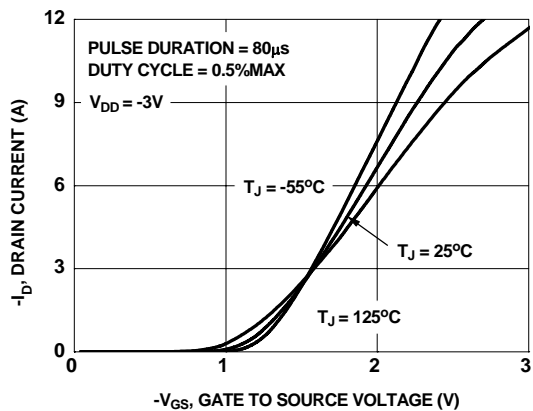


Figure 5. Transfer Characteristics

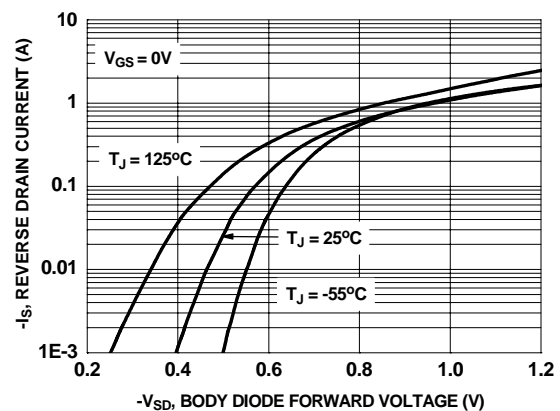


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

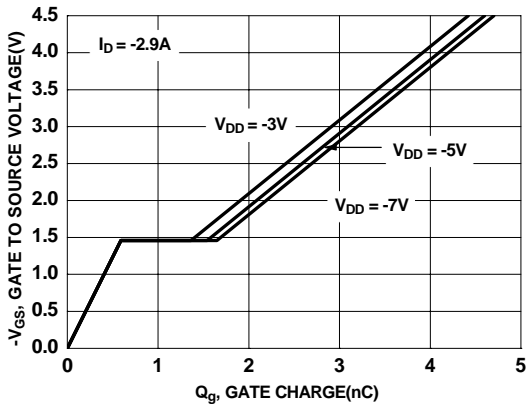


Figure 7. Gate Charge Characteristics

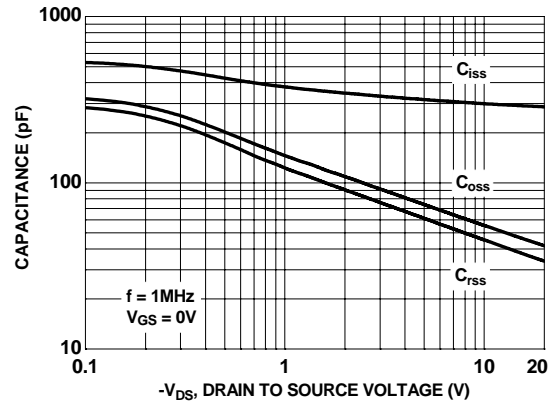


Figure 8. Capacitance vs Drain to Source Voltage

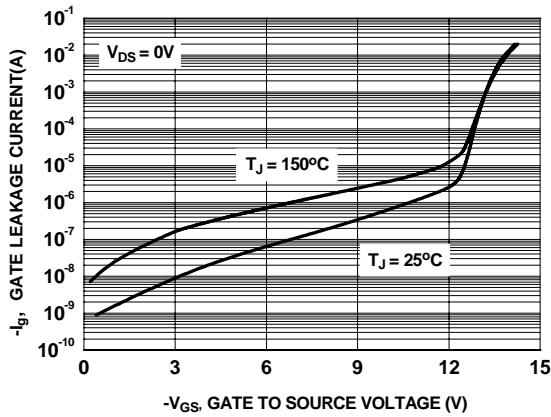


Figure 9. Gate Leakage Current vs Gate to Source Voltage

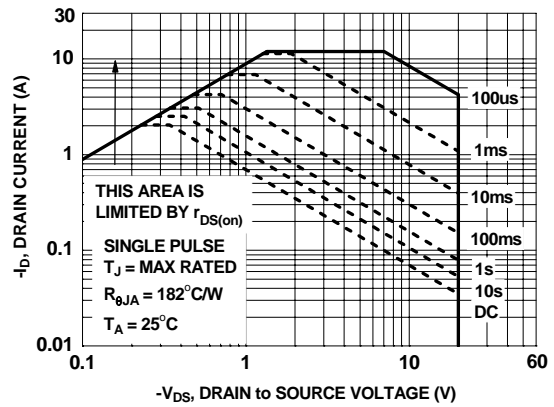


Figure 10. Forward Bias Safe Operating Area

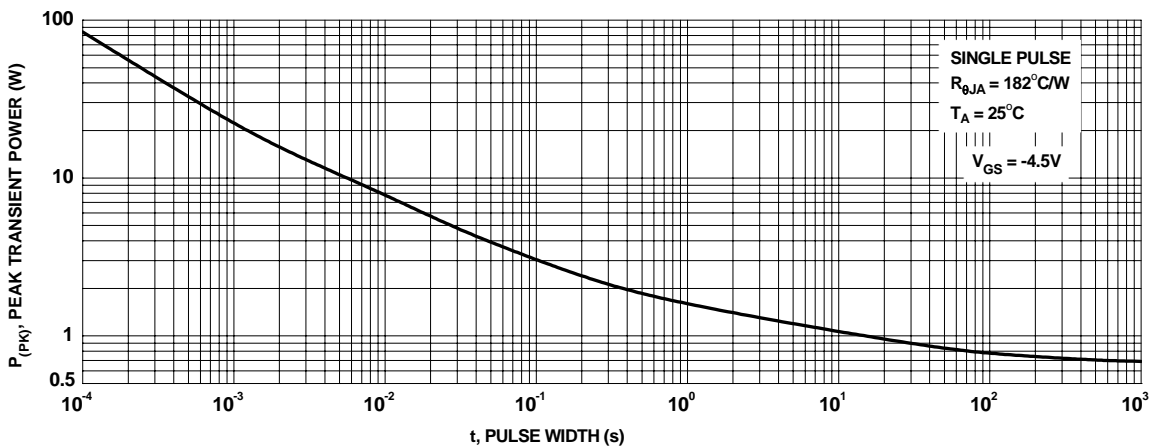


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

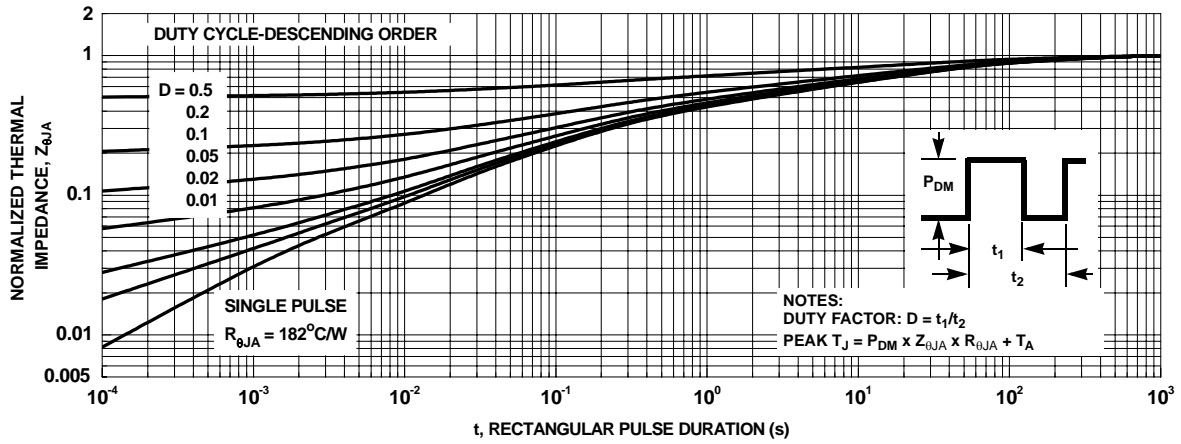
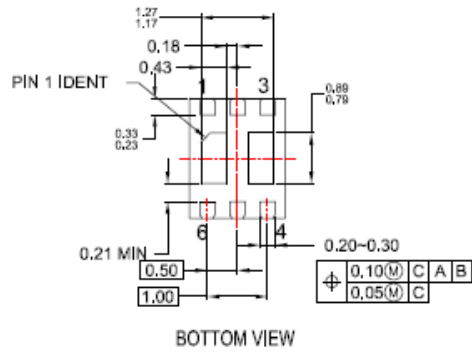
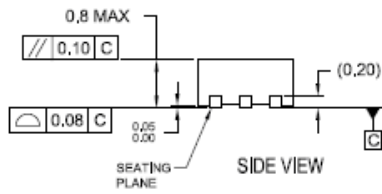
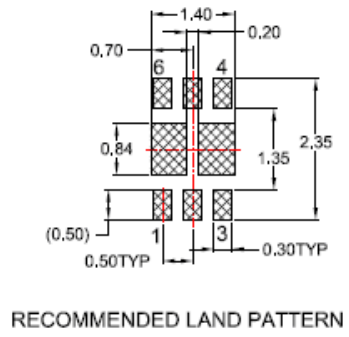
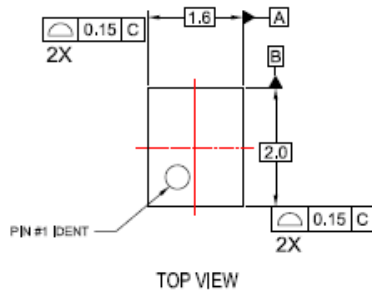


Figure 12. Transient Thermal Response Curve


Dimensional Outline and Pad Layout





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